NON-DISSIPATIVE DC TO DC REGULATOR-CONVERTER STUDY

SEVENTH QUARTERLY REPORT
15 MAY 1966 TO 31 AUGUST 1966

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GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

Prepared by:

Frank L. Raposa
Assistant Project Engineer

Richard K. Seaver
Experimental Engineer

Robert H. Ponsi
Experimental Engineer

Approved By:

William E. Michel
Project Engineer

T. E. O'Brien
Chief Engineer

1.0 ABSTRACT

This report covers the work effort from 15 May 1966 to 31 August 1966. Effort during this phase included both the continuing development of the series of booster power supplies, and the initiating of development of the new series of chopper power supplies. The development effort included the following:

1. Overload protection of the booster regulator converters.
2. Dynamic response of the booster regulator converters.
3. Scaling designs for the booster regulator converters.
4. Initial development of the new chopper regulator converters.

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2.0 PURPOSE

The purpose of this program is to provide concept, techniques, and developed modular circuitry for non-dissipative DC to DC Converters in the power range of 0 to 100 watts.

Major program goals are the maximization of efficiency, simplicity, and reliability, along with minimization of size, weight and response times of the converters.

The circuits are to be modular in concept, so that a minimum of development is required to tailor a circuit to a specific application requirement. The concepts should also allow, inasmuch as practical, for the use of a state-of-the-art manufacturing techniques.

The program is multi-phased, including a study, analysis, and design phase, and a breadboard phase during which the concepts are to be verified by construction and test of eight breadboards.

3.0 INTRODUCTION

The work of the previous quarter included both the continuing development of the booster series of power supplies, and the initiating of development of the new series of chopper power supplies. The work effort included the following:

1. Overload protection of the booster regulator converters. The protection circuits presented in the previous quarterly report provided short circuit protection only. Further development effort was expended to obtain a protection circuit providing both overload and short circuit protection.

2. Dynamic response of the booster regulator converters. Circuit instability can occur because of excessive phase shift in the feedback loop. The series RC compensating circuit used to insure circuit stability, thus affects the dynamic response of the circuit. Empirical investigations were conducted on dynamic response caused by the RC Phase shift networks.

3. Scaling designs for the booster regulator converters. It was recommended in the final project report for the Phase I program that the development effort on the variable frequency chopper regulator converter be discontinued. It was further recommended in that report that the basic control concepts being developed for the booster regulator converters also be applied to a new series of chopper regulator converters. Initial development of this new series of chopper regulator converters has been started. In addition, the use of the unified power stage concept discussed in this report is being applied.

4.0 TECHNICAL DISCUSSION

4.1 Overload Protection of Booster Regulator Converters

Circuit protection investigations were continued in an effort to obtain overload protection in addition to the short circuit protection covered in the previous quarterly report. The circuit shown in Figure 1, is a result of these investigations.

The output terminals of the converter are connected to terminals 1 and 2, the load is connected to terminals 3 and 4, terminal 5 is connected to an auxiliary B+ voltage, and terminal 6 is connected to the output sensing terminal of the voltage regulator. When the converter is turned on, voltage is applied to terminal 5. The voltage developed across resistor R4 is high enough to turn on transistor Q4, which in turn saturates transistors Q2 and Q1. Voltage now appears at terminals 3 and 4, and normal operation now occurs. Under normal operation, the voltage dividing action of resistor R5 and the load sets the emitter of transistor Q3 at a high voltage. The base voltage of transistor Q3 is set just low enough to keep transistor Q3 in a non-conducting state by the voltage divider consisting of resistors R1 and R2. Zener diode ZD1 is normally in a non-conducting state so that the output sensing of the voltage regulator is connected to terminal 3 through resistor R6.

When an overload condition occurs, the increase in load current causes the voltage across resistor R5 to increase. This causes an increase in the voltage at the emitter of transistor Q1 which in turn raises the voltage at the base of transistors Q1 and Q3. Transistor Q3 turns on, and brings transistors Q2 and Q1 out of saturation. With transistor Q1 out of saturation, the voltage that appears from collector to emitter in transistor Q1 increases, thus increasing the voltage at terminal 1. This forces zener diode ZD1 into conduction, causing the voltage regulator now to keep the voltage at terminal 1 constant. Any further overload increases the voltage drop across resistor R5, decreasing the voltage at terminal 3. This limits the load current by bringing transistor Q3 closer to saturation which in turn forces transistors Q2 and Q1 closer to cutoff. When a short circuit condition occurs,

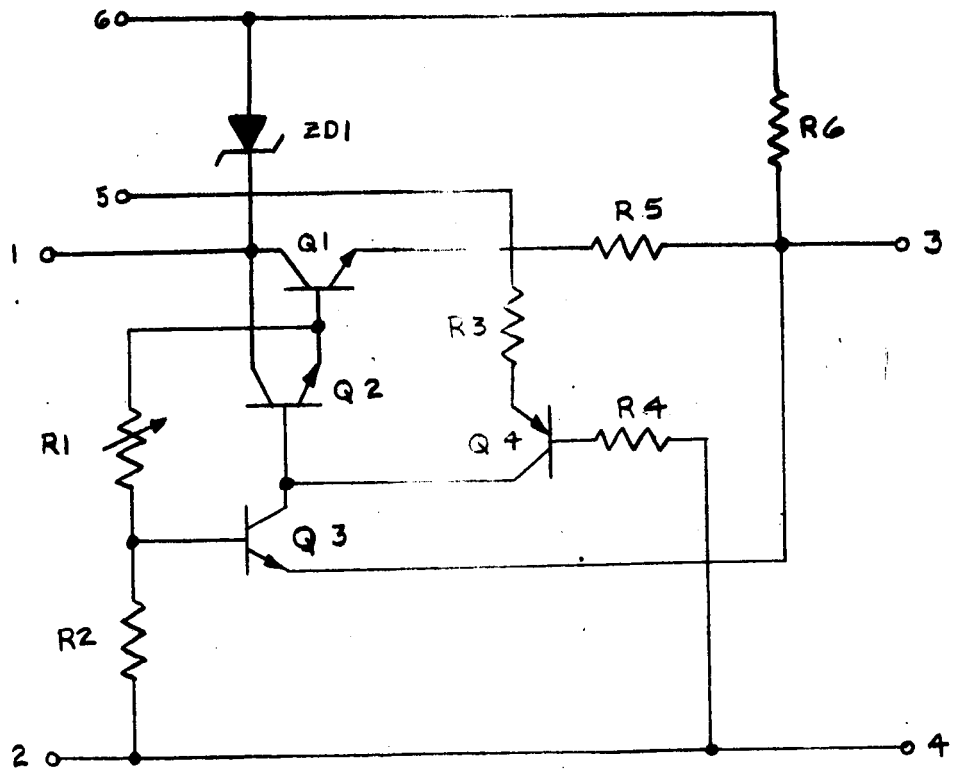


FIGURE 1 - OVERLOAD PROTECTION CIRCUIT

transistor Q3 saturates and drives transistors Q2 and Q1 into a high impedance state, thus isolating the load from the regulator-converter output. When the overload condition is removed, the voltage at terminal 3 increases, turning off transistor Q3, and the circuit automatically returns to the saturated on-state through the starting process described above.

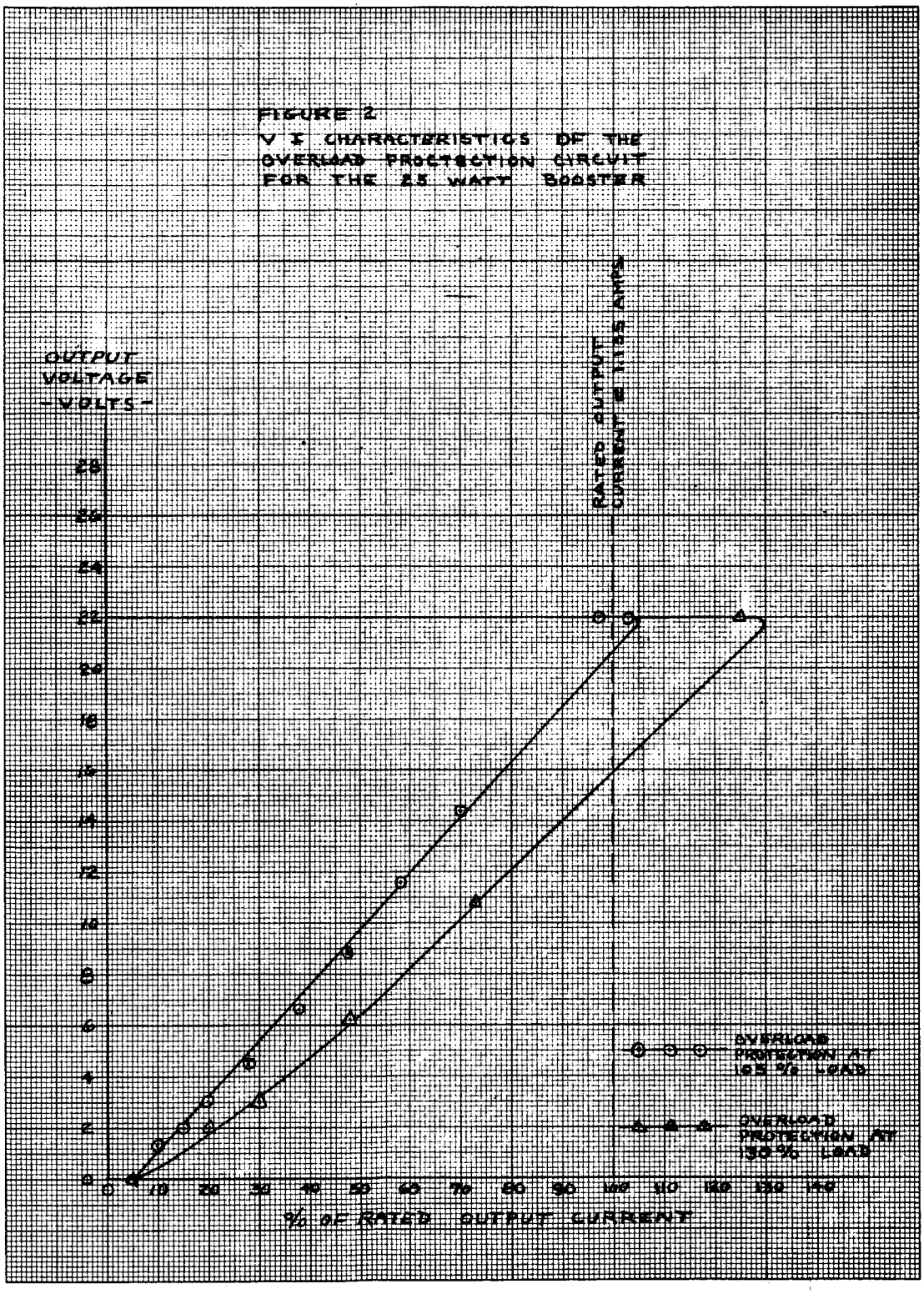
Experimental Data

Breadboard tests were run using the overload protection circuit with the 25 watt booster to determine the characteristics of the overload protection circuit. The tests were conducted using two values for resistor R1, one providing protection for loads in excess of 105% and the other providing protection for loads in excess of 130%.

Figure 2 shows a graph of the load voltage versus per cent of rated output current. With resistor R1 set so transistor Q3 turns on with a 5% overload, it is shown that the output voltage remains constant from no load to approximately 105% load. At this point, the base voltage of transistor Q3 has risen enough to turn on transistor Q3, causing transistors Q2 and Q1 to come out of saturation. The increase in voltage at terminal 1 changes the conduction state of zener diode ZD1 slightly, increasing the voltage regulator sensing current, which causes a small decrease in the voltage at terminal 3. Increasing the load further raises the conduction of transistor Q3 further, which decreases the conduction of transistors Q2 and Q1, and further decreases the output current and voltage. The decrease in output current and voltage is approximately linear from the point at which transistor Q3 begins to conduct, to the short circuit condition. At the short circuit condition, it can be seen that the high impedance state of transistor Q1 allows only about 5% of the rated current to flow.

The per cent load at which the overload protection circuit becomes activated and provides overload protection can be adjusted by varying resistor R1. Increasing resistor R1 initially sets the base of transistor Q3 at a lower voltage. Thus, to turn on transistor Q3, the base voltage of transistor Q1, and thus the voltage drop across resistor R5 must be larger than in the previous case.

FIGURE 2
V I CHARACTERISTICS OF THE
OVERLOAD PROTECTION CIRCUIT
FOR THE 25 WATT BOOSTER



This means that a larger overload must occur before transistor Q3 will turn on and protection will be provided. Note that varying the point at which overload protection is provided has no effect on the output voltage from no load to full load, or at the short circuit condition.

Figure 3 shows the power dissipation in transistor Q1 versus the per cent of rated output current from no load to the short circuit condition for the two overload conditions discussed above. From no load to full load for both cases, the power dissipation increases from essentially zero to approximately one watt at full load. At the point when transistor Q3 is turned on, and transistors Q2 and Q1 are brought out of saturation, the power dissipation in transistor Q1 increases sharply. This is due to the sudden increase in the collector to emitter voltage of transistor Q1 with a high collector current present. With additional overload, the load current, and thus the collector current, decreases. However, the collector to emitter voltage increases at a greater rate than the decreasing collector current. Thus, the power dissipation increases further, reaches a peak, and then falls off as the short circuit condition is approached.

For the case where protection is provided for loads in excess of 105%, the power dissipation in transistor Q1 is about 1.5 watts at 105% of rated output current. The peak power dissipation is approximately 9 watts, and the short circuit power dissipation is about 1.5 watts. With the overload protection circuit set for loads in excess of 130%, the power dissipation is approximately 3 watts at 130% of rated output current, 12 watts at peak power dissipation, and 1.5 watts at short circuit.

Preliminary investigations have shown that the peak power dissipation occurs for both cases when the load voltage and the collector to emitter voltage of transistor Q1 are equal. This is in agreement with maximum power transfer theory. Since maximum power dissipation is substantially higher when overload protection is provided at greater loads, a compromise may have to be made between permissible overload and power dissipation in transistor Q1. Also, the ability of the unit to regulate for loads greater than 100% will be determined by the permissible power dissipation of transistor Q1.

FIGURE 5
SERIES TRANSISTOR POWER DISSIPATION
VERSUS % RATED OUTPUT CURRENT

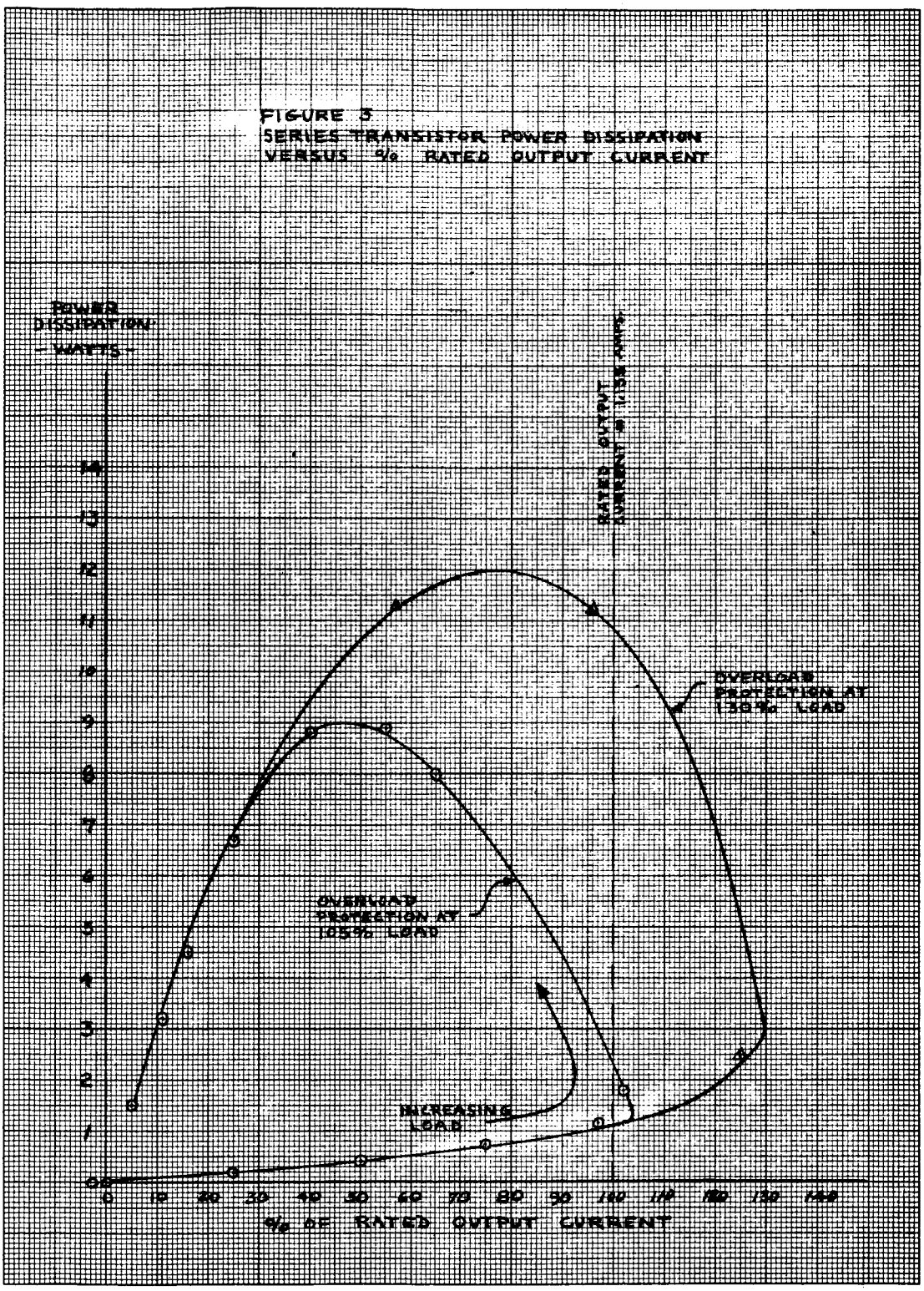


Figure 4 shows a graph of the voltage at the input of the overload protection circuit (terminals 1-2) versus the per cent of rated output current. The overload protection circuit input voltage increases from 22.6 volts at no load, to about 23.5 volts at full load. As expected, it increases suddenly at the point when transistor Q3 turns on, and transistors Q2 and Q1 come out of saturation. This voltage levels off at approximately 25.2 volts when zener diode ZD1 is fully conducting. The effect of the voltage regulator output sensing switch to terminal 1 can be seen from this graph. Switching the sensing to terminal 1 limits the voltage at terminal 1 to 25.2 volts. If switching means were not provided, the voltage at terminal 1 could have risen to almost double its normal value. This would have required power dissipation in transistor Q1 to be more than twice the maximum reached in the previous tests.

4.2 Dynamic Response of the Booster Regulator Converters

Initial investigations have shown that the dynamic regulation and recovery time of the booster regulator converters are dependent upon the resistance and capacitance values in the compensating circuit of the voltage regulator (R28, C9 of the difference amplifier, or R25, C8 of the reference amplifier shown on page 18 of the sixth quarterly progress report.) Breadboard tests were conducted to determine the extent of this dependence.

The circuit shown in Figure 5 was used to produce ramp input voltage changes in the dynamic regulation and recovery time tests. Resistor R1 was set at approximately one ohm. Capacitor C1 was then set so the booster input voltage transient was a ramp change with a slope of one volt per millisecond. With switch S1 open, the booster input voltage was the power supply voltage less the drop across diode D1. When switch S1 was closed, the booster input voltage increased at a rate of one volt per millisecond to the sum of the power supply voltage and the battery voltage less the drop across resistor R1. When switch S1 was opened, the booster input voltage decreased at the same rate to the power supply voltage less the drop across diode D1.

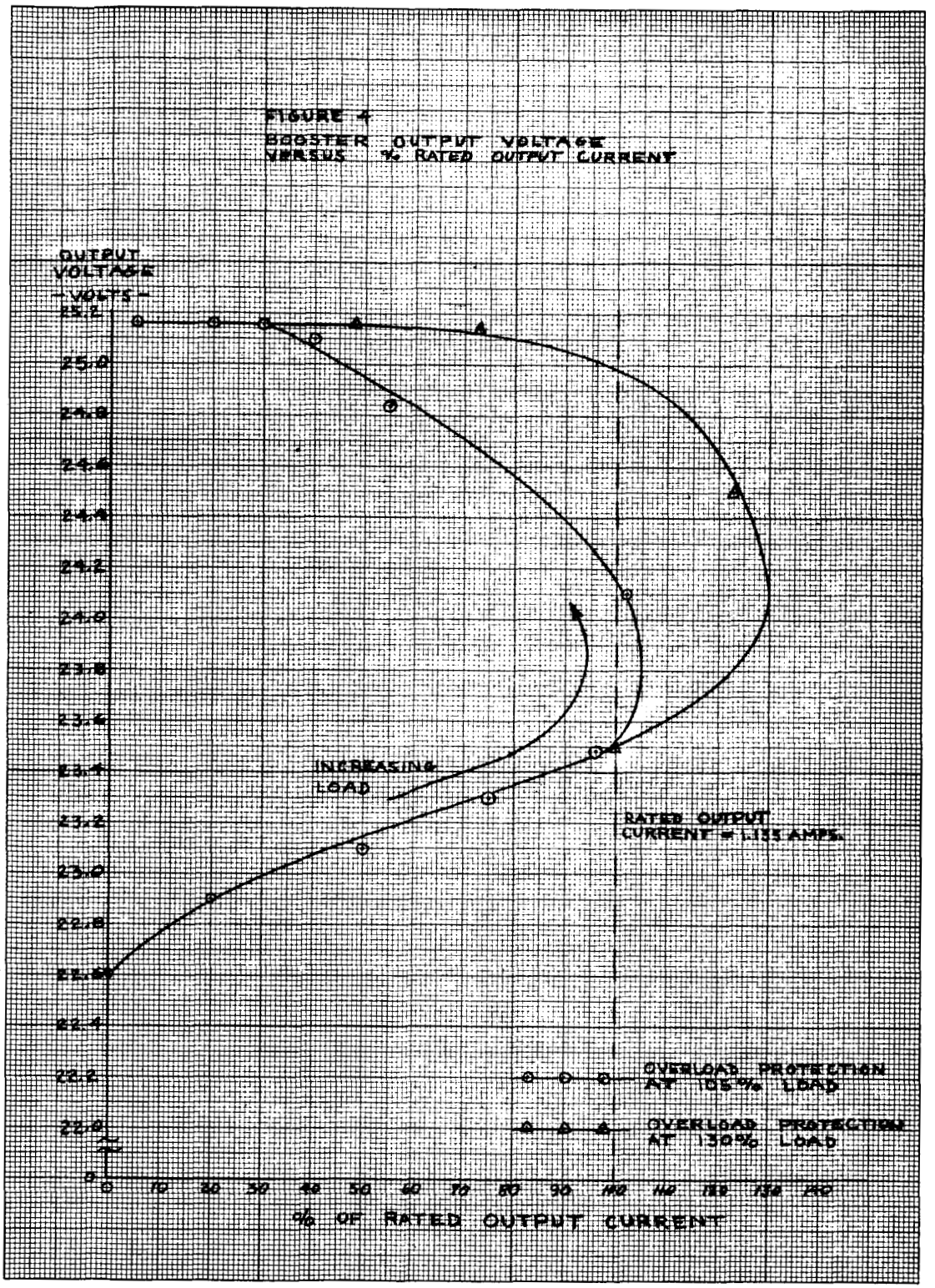


FIGURE 4
BOOSTER OUTPUT VOLTAGE VERSUS % RATED OUTPUT CURRENT
OUTPUT VOLTAGE - VOLTS -
25.2
25.0
24.8
24.6
24.4
24.2
24.0
23.8
23.6
23.4
23.2
23.0
22.8
22.6
22.4
22.2
22.0
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
INCREASING LOAD
RATED OUTPUT CURRENT = 115.5 AMPS.
OVERLOAD PROTECTION AT 105% LOAD
OVERLOAD PROTECTION AT 130% LOAD
% OF RATED OUTPUT CURRENT

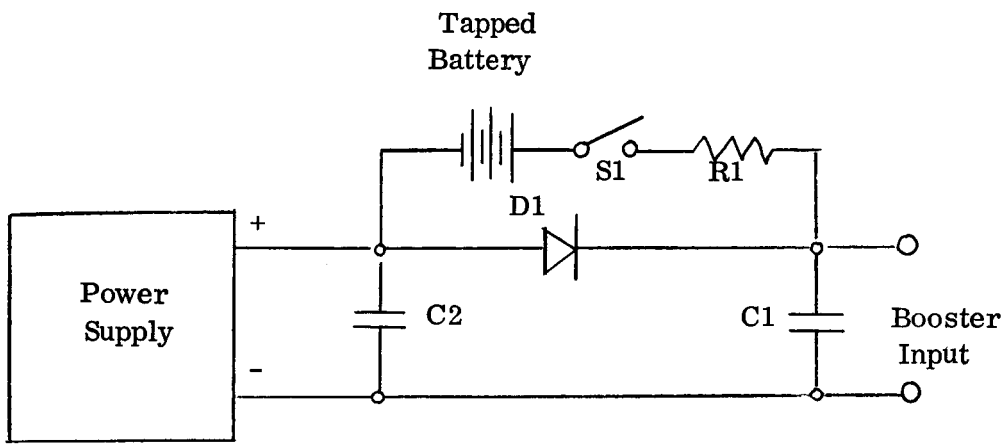


Figure 5. Input Voltage Supply Circuit for Dynamic Regulation and Recovery Time Tests.

Dynamic regulation and recovery time tests were conducted with the 25 watt booster with both the reference amplifier and the difference amplifier voltage regulator circuits. Input voltage ramp changes and load step changes were both considered in these tests. In the initial testing, both the resistance and capacitance in the compensating circuit of the voltage regulator were varied. The results of these tests showed no significant differences in the dynamic regulation or the recovery time of the reference and difference amplifiers. The results of the above tests for the reference amplifier have been presented in Appendix II of this report.

A capacitance of 10 microfarads was selected for the capacitor in the compensating circuit of the voltage regulator. Additional tests were then conducted with the resistance in the compensating circuit as the only variable. The results of these tests can be seen in Figures 6 through 9. These results indicated that a trade off between dynamic regulation and recovery time was necessary. For all transient conditions, the peak voltage excursion decreased with increasing resistance. The recovery times for load changes of 100% load to 75% load, and input voltage changes of 10 volts to 20 volts at full load increased with increasing resistance. A resistance of 3 kilohms was selected as a compromise between dynamic regulation and recovery time.

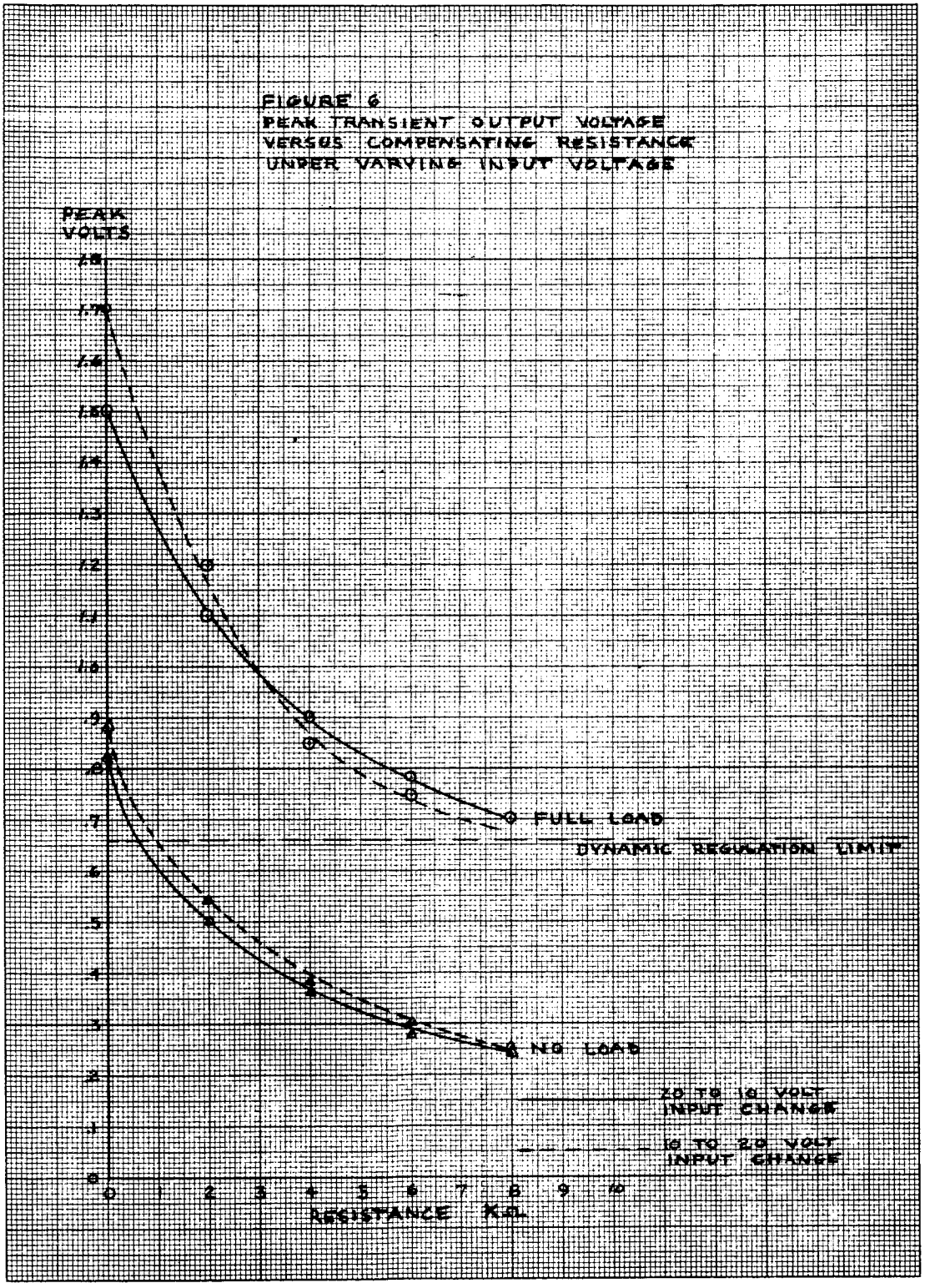
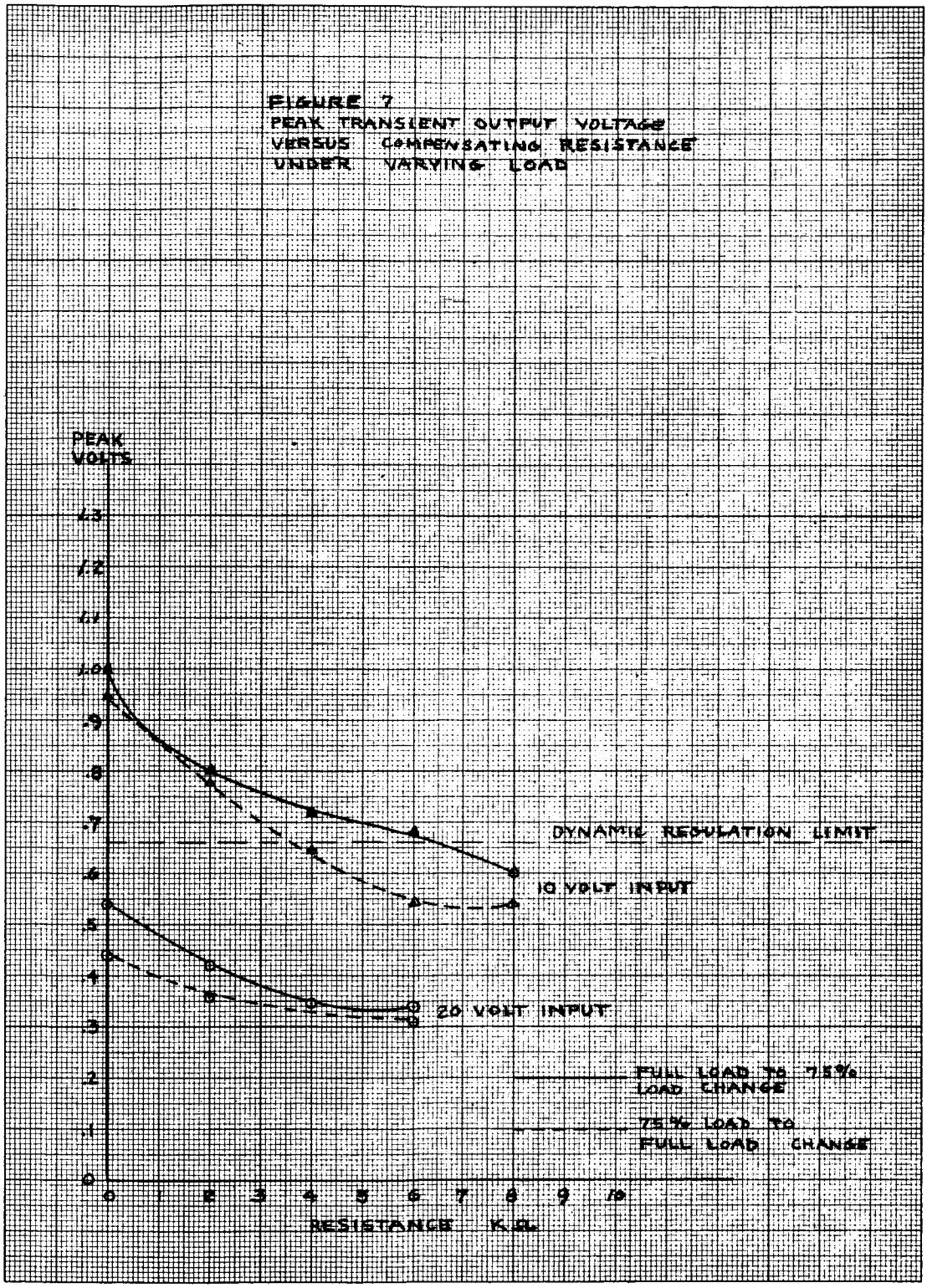


FIGURE 6
PEAK TRANSIENT OUTPUT VOLTAGE
VERSUS COMPENSATING RESISTANCE
UNDER VARYING INPUT VOLTAGE
PEAK VOLTS
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
.9
.8
.7
.6
.5
.4
.3
.2
.1
0
0 1 2 3 4 5 6 7 8 9 10
RESISTANCE KΩ
FULL LOAD
DYNAMIC REGULATION LIMIT
NO LOAD
20 TO 10 VOLT INPUT CHANGE
10 TO 20 VOLT INPUT CHANGE

FIGURE 7
PEAK TRANSIENT OUTPUT VOLTAGE
VERSUS COMPENSATING RESISTANCE
UNDER VARYING LOAD



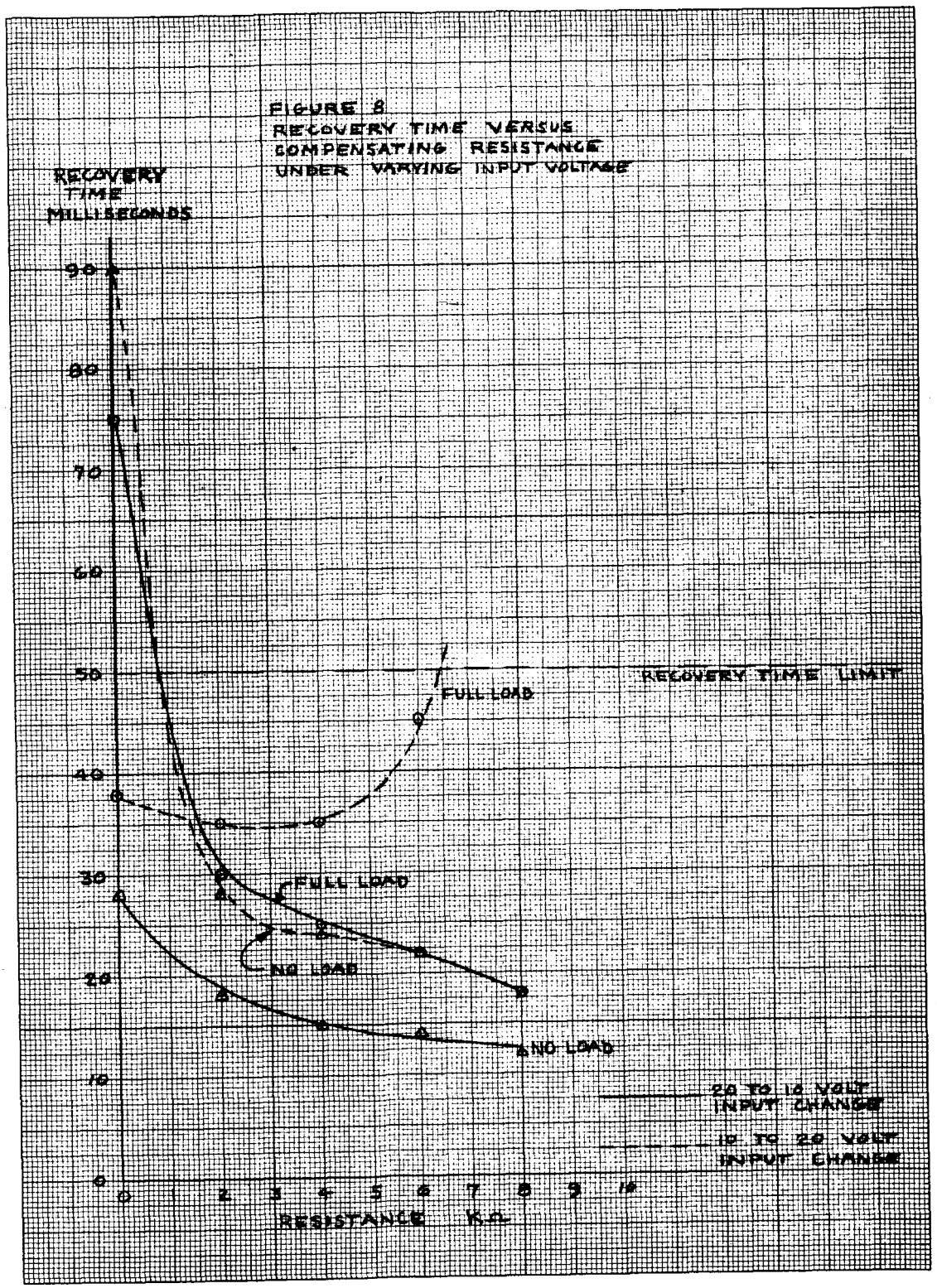


FIGURE 8
RECOVERY TIME VERSUS
COMPENSATING RESISTANCE
UNDER VARYING INPUT VOLTAGE
RECOVERY TIME MILLISECONDS
90
80
70
60
50
40
30
20
10
0
0
1
2
3
4
5
6
7
8
9
10
RESISTANCE K.Ω.
RECOVERY TIME LIMIT
FULL LOAD
FULL LOAD
NO LOAD
NO LOAD
20 TO 10 VOLT INPUT CHANGE
10 TO 20 VOLT INPUT CHANGE

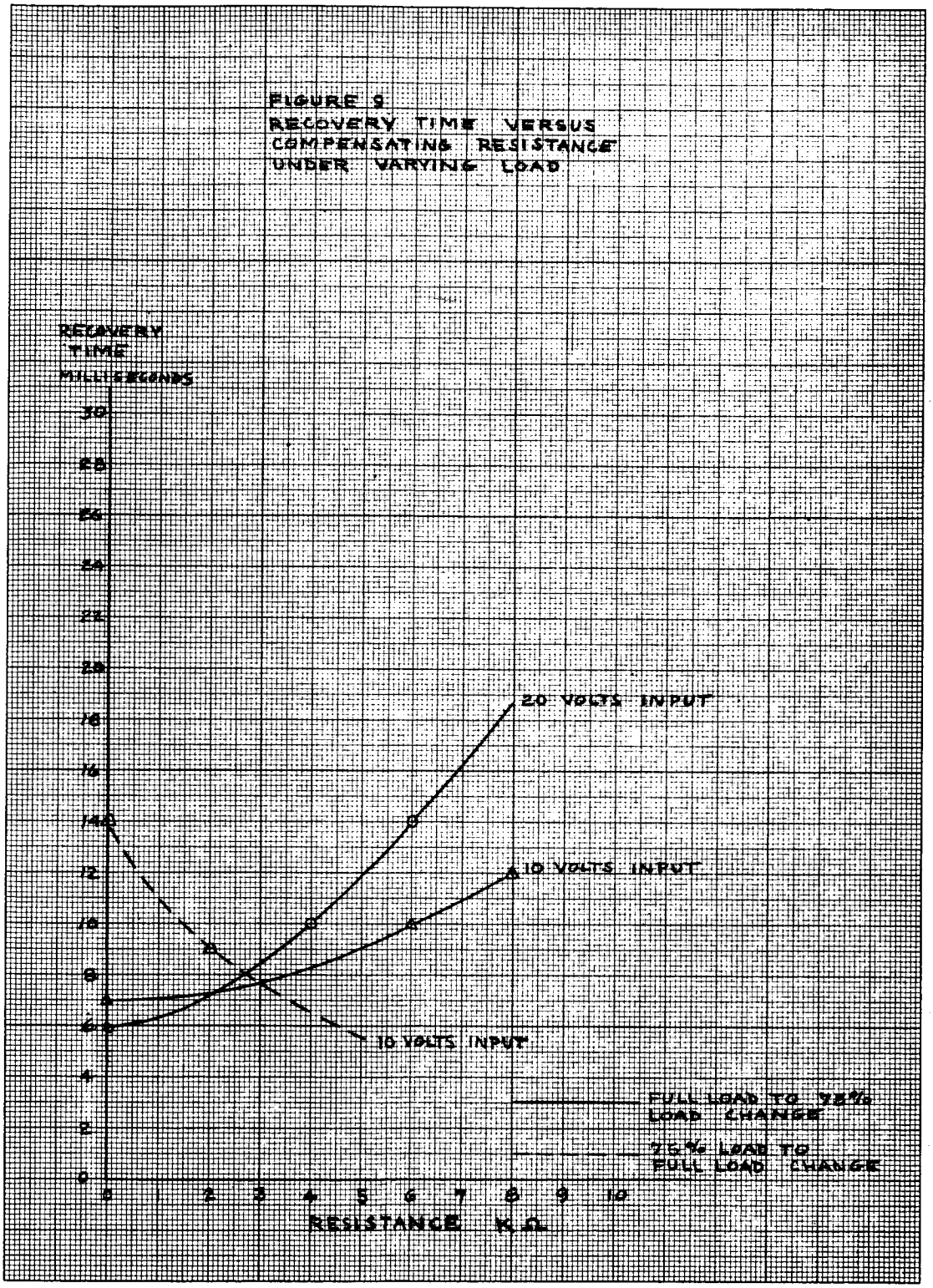


FIGURE 9
RECOVERY TIME VERSUS
COMPENSATING RESISTANCE
UNDER VARYING LOAD
RECOVERY
TIME
MILLISECONDS
30
28
26
24
22
20
18
16
14
12
10
8
6
4
2
0
20 VOLTS INPUT
10 VOLTS INPUT
10 VOLTS INPUT
FULL LOAD TO 75%
LOAD CHANGE
75% LOAD TO
FULL LOAD CHANGE
0
1
2
3
4
5
6
7
8
9
10
RESISTANCE K Ω

Final dynamic regulation and recovery time tests were run on the 25 watt booster to determine the effect of various input voltage levels on the dynamic regulation and recovery time of the unit. Load changes were made at all input voltages, and input voltage transients were made at three different voltage levels at no load and full load conditions. Dynamic regulation and recovery time were recorded for each case. The results of these tests have been shown in Table 1. The dynamic regulation readings were peak transient voltage values. The recovery time was defined as the time for the output voltage to return to 1% of its original value measured from the beginning of the output voltage transient.

Both the peak transient voltage and the recovery time decreased as the input voltage increased for step load changes. For a load change from 100% to 75% of the rated load, the peak transient voltage was 0.85 volts at 10 volts input. This decreased to 0.50 volts at 16 volts input and remained constant for further increases in input voltage. The recovery time for this case was less than or equal to 10 milliseconds for all input voltages 12 volts or greater. For a load change from 75% to 100% of rated load, the peak transient voltage at 10 volts input was 0.70 volts. This decreased to 0.25 volts at 17 volts input and remained constant for further increases in input voltage. The recovery time for for this case was less than 10 milliseconds for all input voltages 12 volts or greater. For input voltage changes at no load and full load conditions, the peak voltage transient and the recovery time decreased as the low input voltage level was raised for all cases with one exception. For the no load condition with input voltage changes from low voltage to 20 volts, the peak voltage transient and recovery time were smallest for a change of 11.2 volts to 20 volts. In this case, since the peak voltage transient did not reach 1% of the output voltage, the recovery time was considered to be negligible. Note that for no load input voltage changes, two cases exist where the input voltage limits of the booster have been exceeded. This was due to the state of the charge of the battery, and the fact that the battery voltage was adjustable only in steps of approximately two volts.

Table I

25 Watt Booster/Reference Amplifier Dynamic Response Data

Lead	Input Volts	Dynamic Response	
		Dynamic Regulation Peak Volts	Recovery Time Milliseconds
E→3/4	10	+0.85	24
	11	+0.75	14
	12	+0.70	10
	13	+0.65	10
	14	+0.60	<10
	15	+0.55	<10
	16	+0.50	<10
	17	+0.50	<10
	18	+0.50	<10
	19	+0.50	<10
	20	+0.50	<10
3/4→F.L.	10	-0.70	22
	11	-0.65	15
	12	-0.60	<10
	13	-0.50	<10
	14	-0.50	<10
	15	-0.40	<10
	16	-0.30	<10
	17	-0.25	<10
	18	-0.25	<10
	19	-0.25	<10
	20	-0.25	<10
N. L.	9.5→20.6	+0.30	12
	11.2→20	+0.10	--
	13.25→20	-0.25	30
N. L.	20.6→9.5	+0.70	50
	20.0→11.2	+0.60	18
	20.0→13.25	+0.55	23
F. L.	10.5→20	-1.0	40
	12.8→20	-0.40	28
	15 20	-0.30	24
F. L.	20→10.5	+1.25	38
	20→12.8	+0.70	24
	20→15	+0.50	22

Dynamic response design goals
Dynamic regulation: ± 0.66 volts
Recovery time" 50 milliseconds

For input voltage changes, two cases occurred where the peak voltage transient was abnormally large. For the full load condition with input voltage changes of 10.5 to 20 volts and 20 to 10.5 volts, the output voltage transients were 1.0 volt and 1.25 volts respectively. The recovery time did not exceed 50 milliseconds for any of the transients investigated. In three cases, however, it did approach this maximum. For full load, 10.5 to 20 volts input change, the recovery time was 40 milliseconds. For full load, 20 to 10.5 volts input change, the recovery time was approximately 38 milliseconds. For the no load condition, 20.6 to 9.5 volt input change, the recovery time was approximately 50 milliseconds. Note, however, that this was one of the cases where the input voltage requirements of the booster were exceeded.

4.3 Scaling Designs - Booster Regulator Converters

Scaling designs for the booster regulator converters were started during the past quarterly period. Breadboards for all power levels have been constructed. The appropriate converter protection circuits for each of the power levels also have been constructed. Only final definition of the voltage regulator circuit remains. Preliminary breadboard tests to date have shown the performance of these circuits to be similar to the Phase I program breadboards.

4.4 New Chopper Development

Circuit Description:

Investigations were initiated into the development of a new set of chopper regulator converters using the control concepts developed for the booster regulator converters. The new circuit configuration, shown in Figure 10, is similar in operation to the booster regulator converters.

Fundamentally, the chopper is a power stage, made up of transistor Q8, diode D2, inductor L1 and capacitor C6; and a control circuit consisting of a current feedback transformer, reset and trigger transistors, a Schmitt trigger, and a ramp generator. A detailed description of the power stage is given in Appendix I

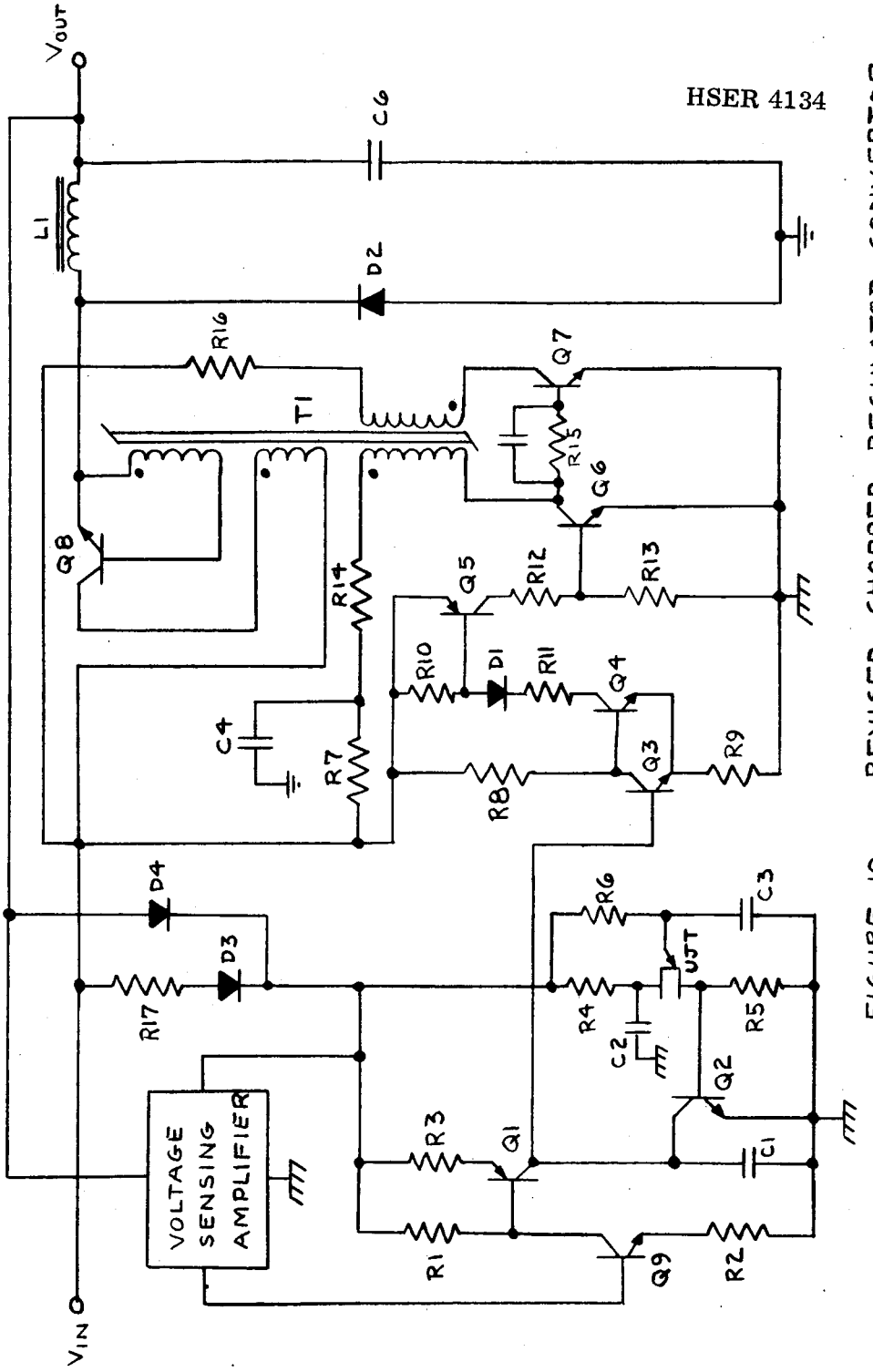


FIGURE 10 . REVISED CHOPPER REGULATOR CONVERTOR

in terms of the unified power stage concept. The chopper control circuitry functions identically to the booster control circuitry, and the two differ only in current and voltage levels and pulse width control required. A starting circuit, consisting of diodes D3 and D4 and resistor R17, is the only addition to the control circuitry. During starting, R17 and D3 conduct supplying unregulated voltage to start the oscillator and ramp generator; thus starting the chopper and producing a voltage at the output. When this voltage reaches a value higher than that supplied by R17 and D3, D4 conducts, supplying a regulated voltage and back biasing D3.

Development Effort:

The prime problem encountered to date in the development of new chopper converter regulators is achieving reliable operation as the input voltage magnitude approaches the output voltage magnitude. Under this condition, with the control circuitry being used, the reset time of the current feedback transformer becomes very short, thus requiring large voltages to reset the driver core. The increased voltage requirement gives rise to two problems:

1. It requires more pulse power in the reset circuitry.
2. It raises the emitter-base voltage seen by the power transistor during reset.

For example, for an input voltage of 10 volts and an output voltage of 9 volts, the reset time is less than 10% of the total period. This means that during reset the emitter-base junction could be subjected to as much as 12 volts, or 4 volts over the rated value for the components presently being used.

It was decided that the limits on the input voltage or output voltage would have to be changed to alleviate this problem. The following limits were chosen:

10 watt chopper	12 to 20 volt input,	9 volt output
25 watt chopper	12 to 20 volt input,	9 volt output
50 watt chopper	14 to 20 volt input,	11 volt output
100 watt chopper	24 to 33 volt input,	20 volt output

With these changes, the choppers would be operable, but it should be noted that the peak emitter base voltages are still close to the maximum rated values of standard high frequency power transistors.

Supplying a regulated voltage for the control circuitry presents another problem; a regulated voltage can be obtained by regulating the input voltage or by using the already regulated output voltage. Efficiency considerations indicate that the output should be used, but, because there is no voltage at the output until the control circuitry is running, a starting circuit is necessary.

5.0 CONCLUSIONS AND RECOMMENDATIONS

A protection circuit has been established which provides overload protection in addition to short circuit protection. However, thermal considerations should limit the use of this circuit to the lower power levels only. It is recommended that this overload protection circuit be used at the 10 watt and 25 watt power levels only, and that the short circuit protection circuit presented in the previous quarterly report be used at the 50 watt and 100 watt power levels.

The dynamic regulation and recovery time have been shown to be dependent on the booster input voltage. For input voltages greater than approximately 13 volts input, the dynamic regulation design goal requirement of $\pm$ 0.66 volts has been met with the 25 watt breadboard tested. The recovery time limit of 50 milliseconds has been met for all conditions tested. For input voltages greater than 13 volts, the recovery time for step load changes has been shown to be less than 10 milliseconds.

The preliminary development of the new chopper regulator converter conducted to date indicates that successful operation can be obtained with the limited input voltage range described in this report.

6.0 PROGRAM FOR NEXT INTERVAL

During the next quarterly period, effort will be directed in the following areas:

A. Complete the scaling designs of the booster regulator converters.

B. Complete the development effort of the new modified chopper regulator converters.

C. Initiate and complete the scaling designs of the modified chopper regulator converters.

D. Obtain performance data for all breadboards.

7.0 BIBLIOGRAPHY

The references used during this past quarter and in the preparation of this report are listed below:

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8.0 CONFERENCES

A conference was held at NASA Goddard on July 20, 1966. In attendance was Mr. E. Pascuitti representing NASA, and Mr. F. Raposa representing HSED. The revised circuit protection scheme providing both overload and short circuit protection was covered. It was agreed that this revised circuit be used at the 10 watt and 25 watt levels, and that the original circuit protection scheme presented in the sixth quarterly report be used at the 50 watt and 100 watt levels.

9.0 NEW TECHNOLOGY

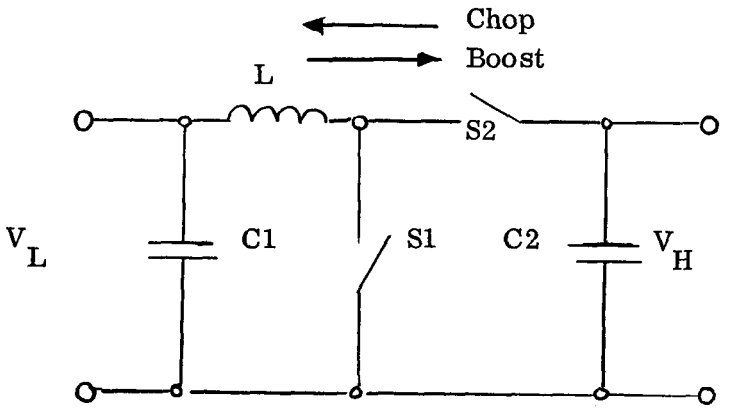
Not applicable during this report period.

APPENDIX I

UNIFIED POWER STAGE CONCEPT

Unified Power Stage Concept

The circuit shown in Figure I-1 can act as a booster or chopper of DC voltage depending upon the direction of power flow within the circuit.



S1 is closed when S2 is open, S1 is open when S2 is closed; both S1 and S2 are bidirectional switches

Figure I-1 - Unified Power Stage Concept.

For boosting action, the input voltage is supplied to the V_L terminals, and a voltage higher than V_L is produced at V_H. In operation, switch S1 closes with switch S2 open, and current builds up linearly through inductor L. After a given interval, switch S1 opens, and switch S2 closes. This adds the voltage induced in the inductor L to the source voltage creating an output voltage higher than the input voltage. During the next half cycle switch S2 opens and S1 closes, so that inductor L is charging up, and capacitor C2 is discharging into the load. It can be shown that the boost output is given by:

$$V_o = \frac{V_L}{1-\theta}$$ where θ is the conduction angle of switch S1

For chopping action the source voltage is supplied to the V_H terminals, and the output is taken at V_L. In operation, switch S2 is closed and switch S1 is open; as with the booster, the current

builds up in choke L. After a given interval S2 opens and S1 closes. Now the voltage induced in choke L is directly across the load. It can be shown that the chopped output is given by:

$V_o = V_i \phi$ where ϕ is the conduction angle of switch S2.

Note that in the above discussion, the current flow through switches S1 and S2 must be bidirectional for the given circuit to provide either boosting or chopping action.

For practical operation, switches S1 and S2 must be replaced with semiconductors which are unidirectional devices. For chopper action, switch S1 is replaced by a diode and S2 is replaced by a transistor as shown in Figure I-2.

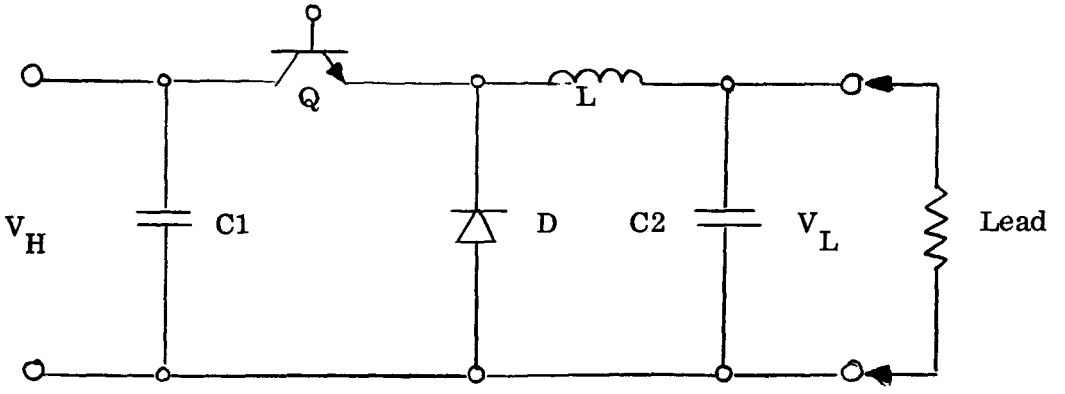


Figure I-2 Chopper Power Stage

Transistor Q is switched by external circuitry, and diode D is switched by the polarity reversals across the inductor L. With transistor Q on, diode D is back biased by the source voltage; when fransistor Q is off, diode D is forward biased by the induced voltage across inductor L.

For booster action, switch S1 is replaced by a transistor, and switch S2 is replaced by a diode as shown in Figure I-3.

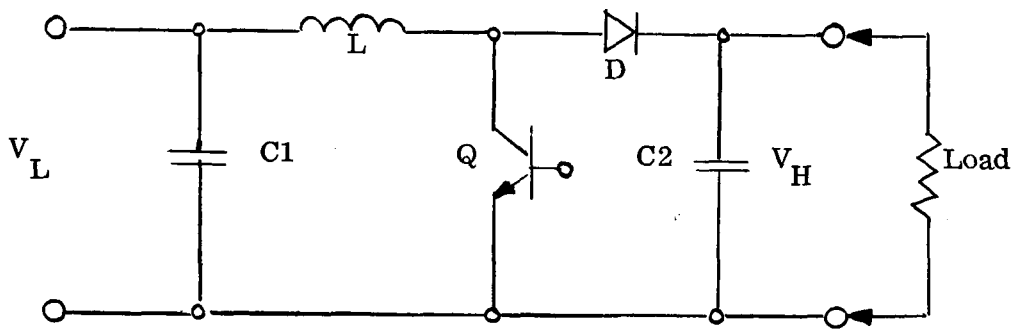
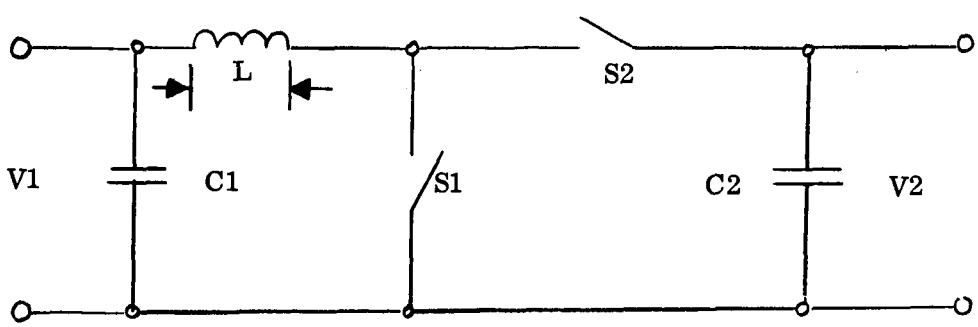


Figure I-3 Booster Power Stage

Transistor Q is switched on and off by external circuitry and diode D is switched by the changing bias voltage caused by the switching action of transistor Q. With transistor Q on, D is back-biased by the output voltage; when transistor Q is off, diode D is forward biased by the induced voltage in choke L and the supply voltage.

Derivation of Chopper-Booster Output Voltage



Conditions:

t_1 and E_1 are the time and voltage across L when S1 is conducting.

t_2 and E_2 are the time and voltage across L when S2 is conducting.

Using the basic equation for induced voltage,

1) $E = \frac{L \Delta i}{\Delta t}$ or $E \Delta t = L \Delta i$ Because the total volt-second product across inductor L must equal zero,

2) $E_1 \Delta t_1 = E_2 \Delta t_2 = L \Delta i_1 = L \Delta i_2$

3) During Δt_1, $V_1 = E_1$ or $E_1 = V_1$

4) During Δt_2, $V_2 = V_1 + E_2$ or, $E_2 = V_2 - V_1$

Substituting equations 3 and 4 into equation 2,

5) $V_1 \Delta t_1 = (V_2 - V_1) \Delta t_2$ or $V_1 (\Delta t_1 + \Delta t_2) = V_2 \Delta t_2$

defining T as the total period $\Delta t_1 + \Delta t_2$

$$V_2 = \frac{V_1 T}{\Delta t_2}$$

This equation is the general form for either the booster or the chopper; for booster action V_2 is the output voltage and V_1 is the input voltage; therefore:

$$V_o = V_i \frac{T}{\Delta t_2} \quad \text{and} \quad \Delta t_2 = T - \Delta t_1 \text{ so,}$$

$$V_{OUT} = V_{IN} \frac{T}{T - \Delta t_1} = \frac{V_{IN}\ 1}{1 - \frac{\Delta t_1}{T}} = V_{IN} \frac{1}{1-0}$$

where θ is the conduction angle of switch S1.

For chopping action, V_2 is the input voltage and V_1 is the output voltage, so:

$$V_i = Vo \frac{T}{t_2} \quad \text{or} \quad Vo = Vi \frac{t_2}{T} = Vi\ \phi$$

where ϕ is the conduction angle of switch S2.

APPENDIX II

DYNAMIC RESPONSE TESTS FOR THE 25 WATT BOOSTER

FIGURE 11

PEAK TRANSIENT OUTPUT VOLTAGE VERSUS COMPENSATING RESISTANCE UNDER VARYING INPUT VOLTAGE AT FULL LOAD CONDITION

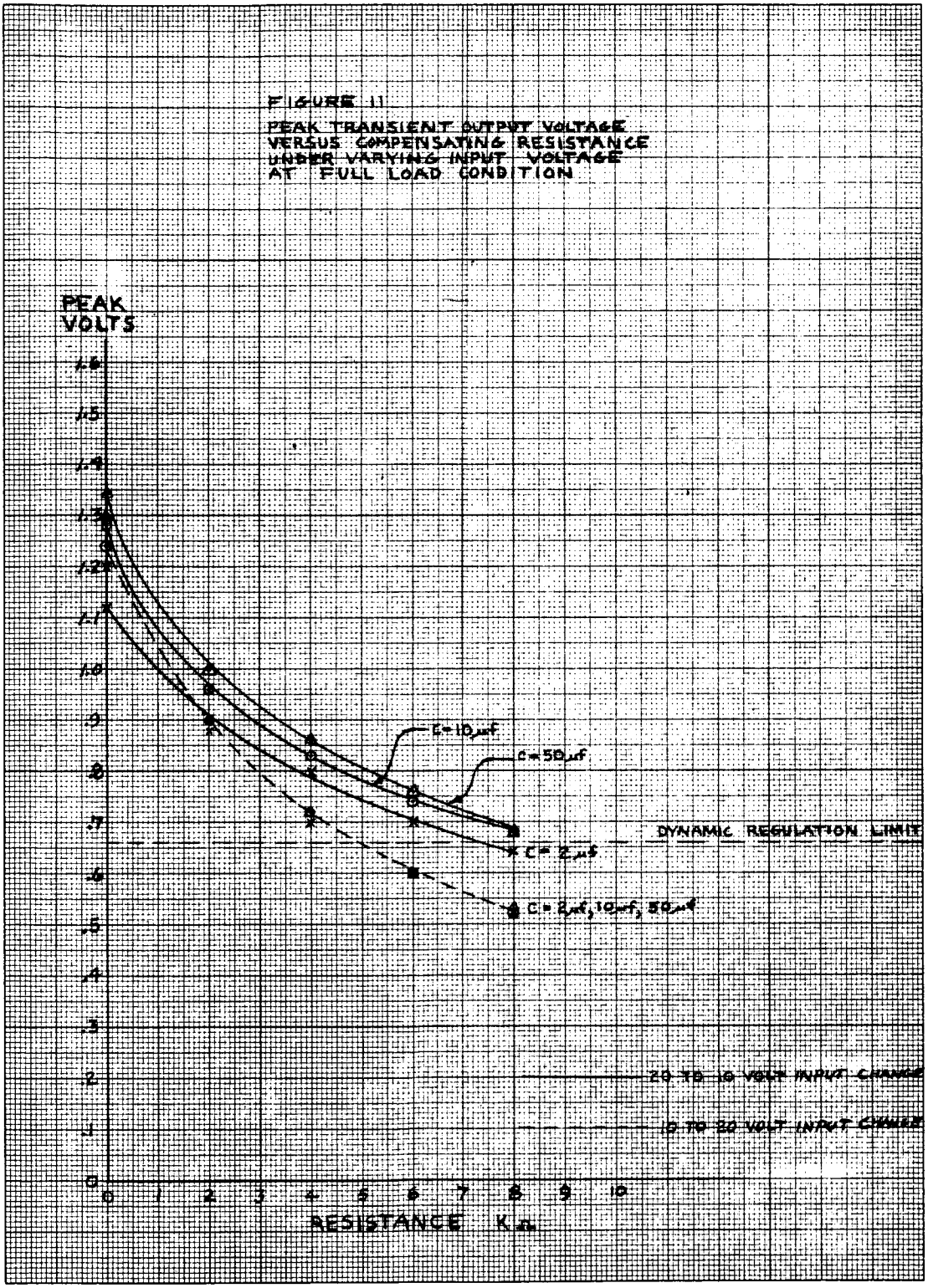
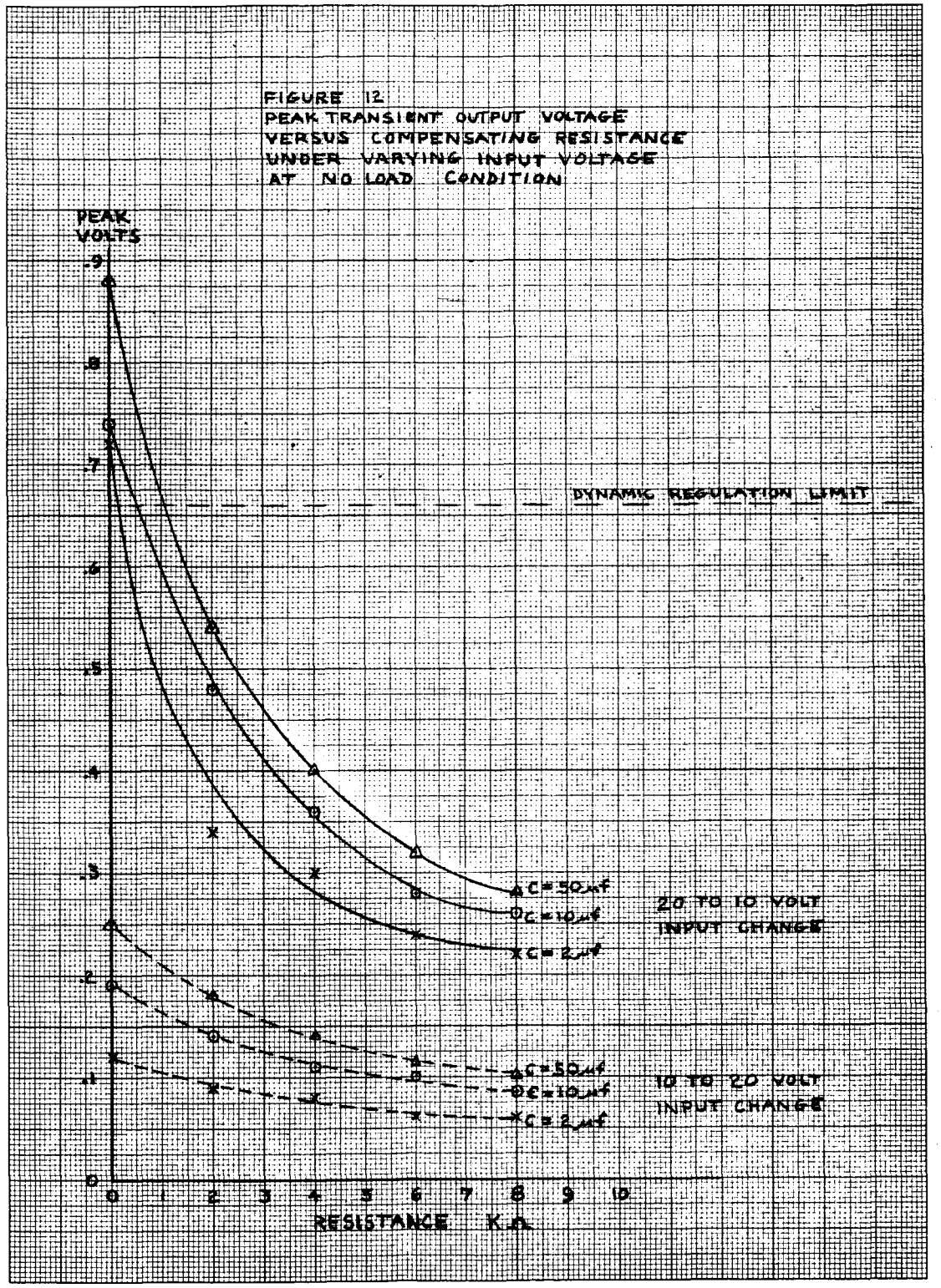


FIGURE 12.
PEAK TRANSIENT OUTPUT VOLTAGE
VERSUS COMPENSATING RESISTANCE
UNDER VARYING INPUT VOLTAGE
AT NO LOAD CONDITION



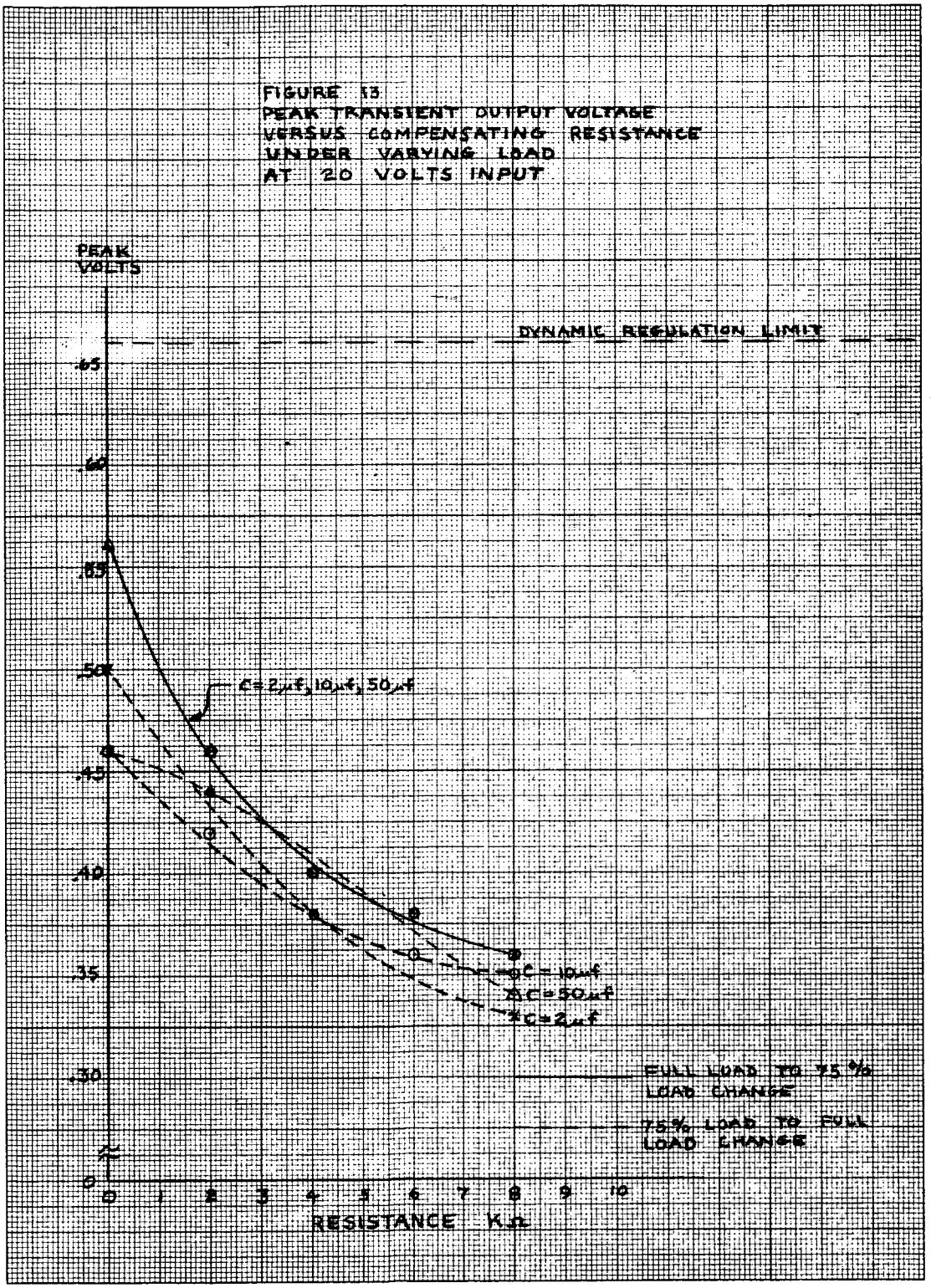


FIGURE 33
PEAK TRANSIENT OUTPUT VOLTAGE
VERSUS COMPENSATING RESISTANCE
UNDER VARYING LOAD
AT 20 VOLTS INPUT
PEAK VOLTS
DYNAMIC REGULATION LIMIT
.65
.60
.55
.50
.45
.40
.35
.30
C=2μf, 10μf, 50μf
C=10μf
C=50μf
C=2μf
FULL LOAD TO 75% LOAD CHANGE
75% LOAD TO FULL LOAD CHANGE
0 1 2 3 4 5 6 7 8 9 10
RESISTANCE KΩ

FIGURE 14
PEAK TRANSIENT OUTPUT VOLTAGE VERSUS COMPENSATING RESISTANCE UNDER VARYING LOAD AT 10 VOLTS INPUT

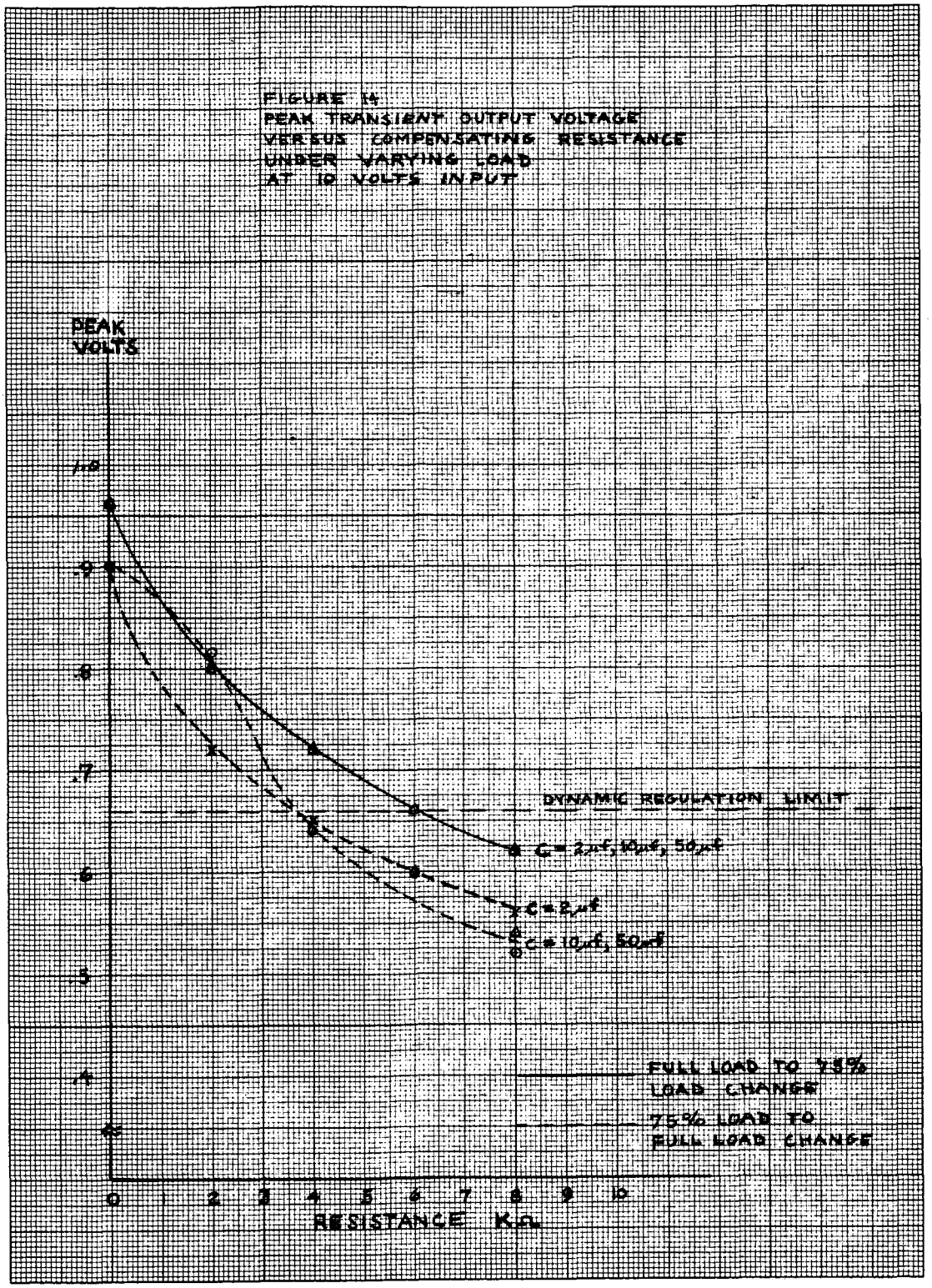
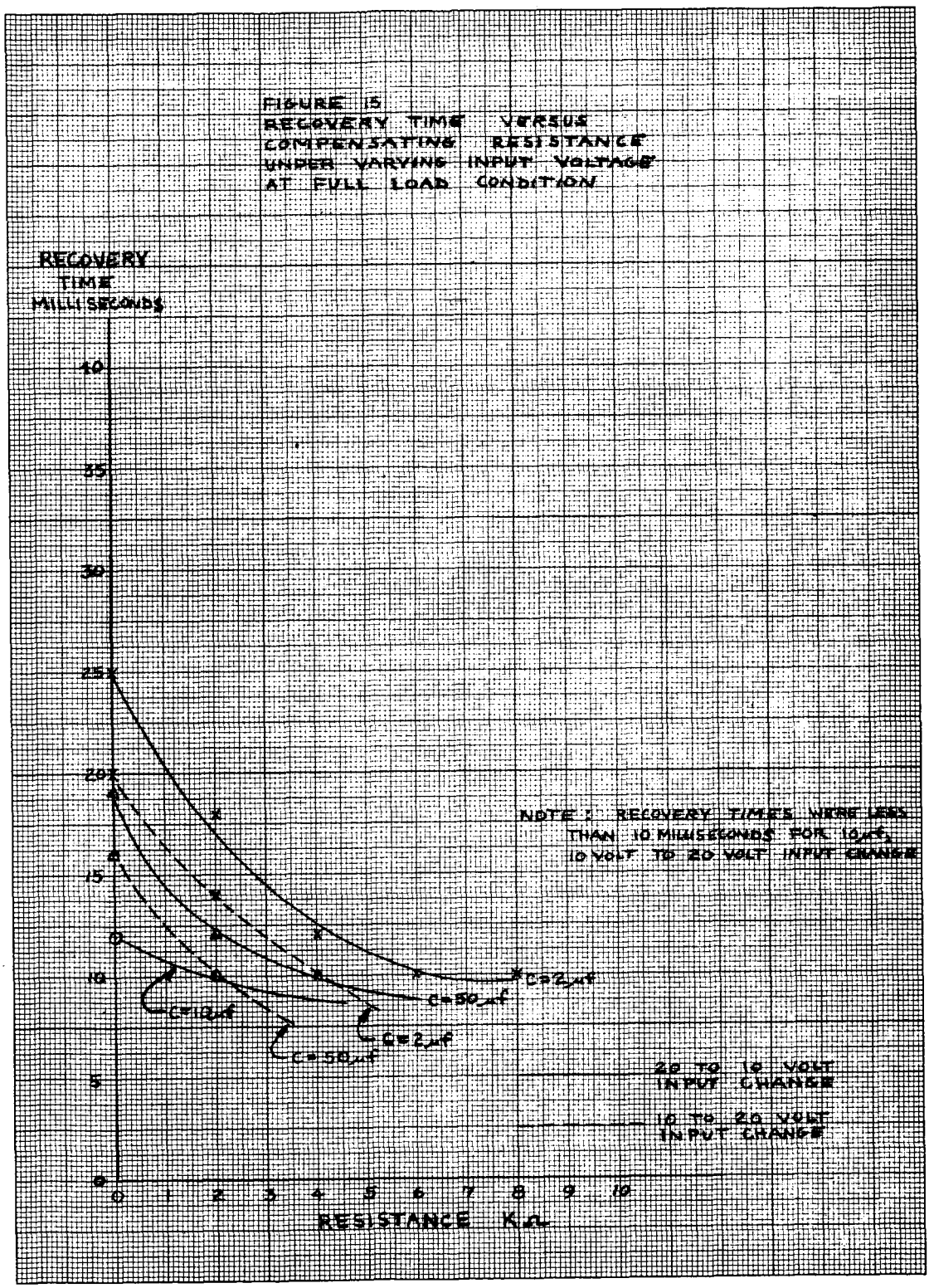


FIGURE 15
RECOVERY TIME VERSUS
COMPENSATING RESISTANCE
UNDER VARYING INPUT VOLTAGE
AT FULL LOAD CONDITION



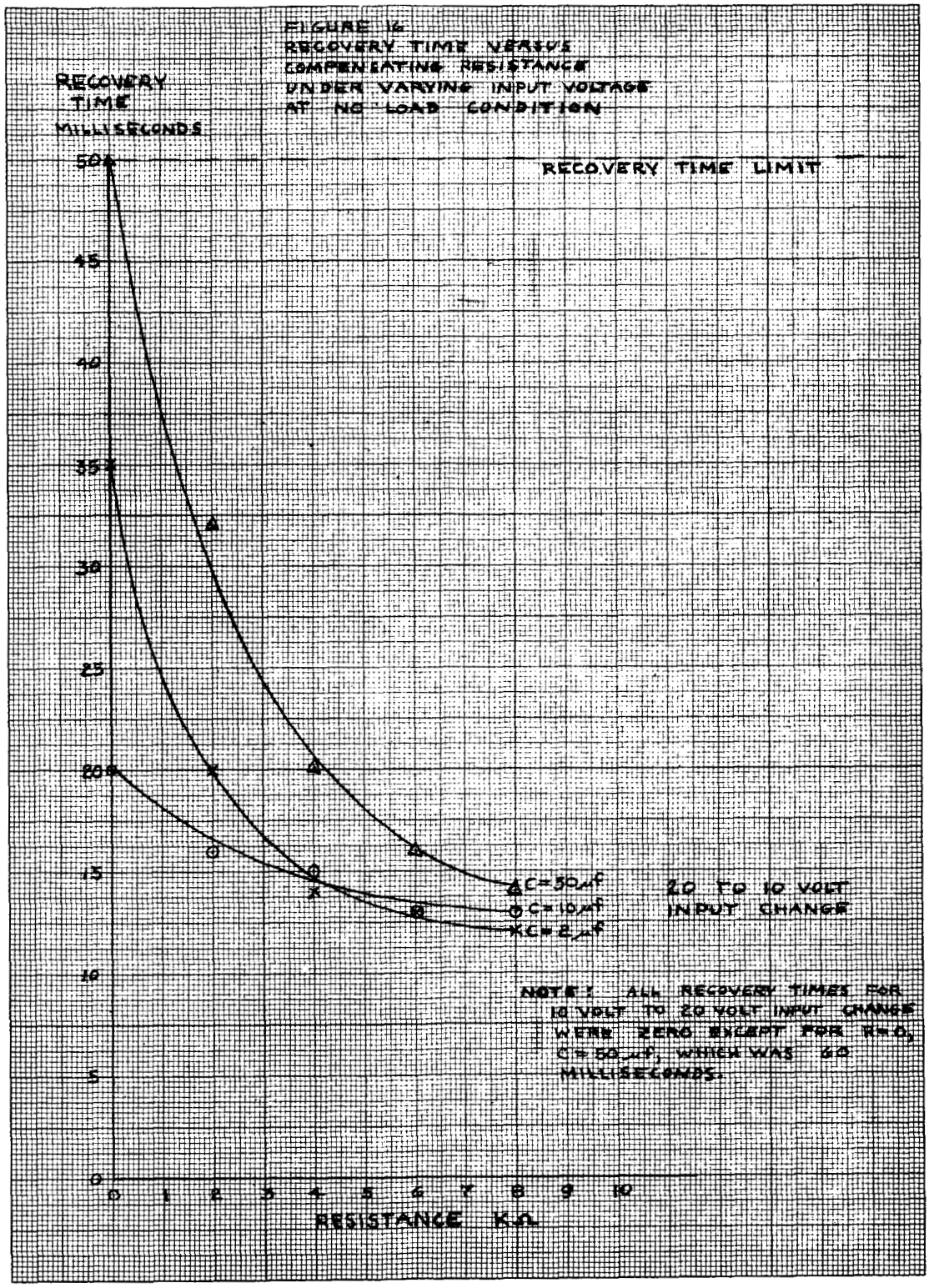


FIGURE 16
RECOVERY TIME VERSUS
COMPENSATING RESISTANCE
UNDER VARYING INPUT VOLTAGE
AT NO LOAD CONDITION
RECOVERY TIME
MILLISECONDS
50
45
40
35
30
25
20
15
10
5
0
RECOVERY TIME LIMIT
C=50μf
C=10μf
C=2μf
20 TO 10 VOLT
INPUT CHANGE
NOTE: ALL RECOVERY TIMES FOR
10 VOLT TO 20 VOLT INPUT CHANGE
WERE ZERO EXCEPT FOR R=0,
C=50μf, WHICH WAS 60
MILLISECONDS.
0 1 2 3 4 5 6 7 8 9 10
RESISTANCE KΩ

FIGURE 17
RECOVERY TIME VERSUS
COMPENSATING RESISTANCE
UNDER VARYING LOAD
AT 20 VOLTS INPUT

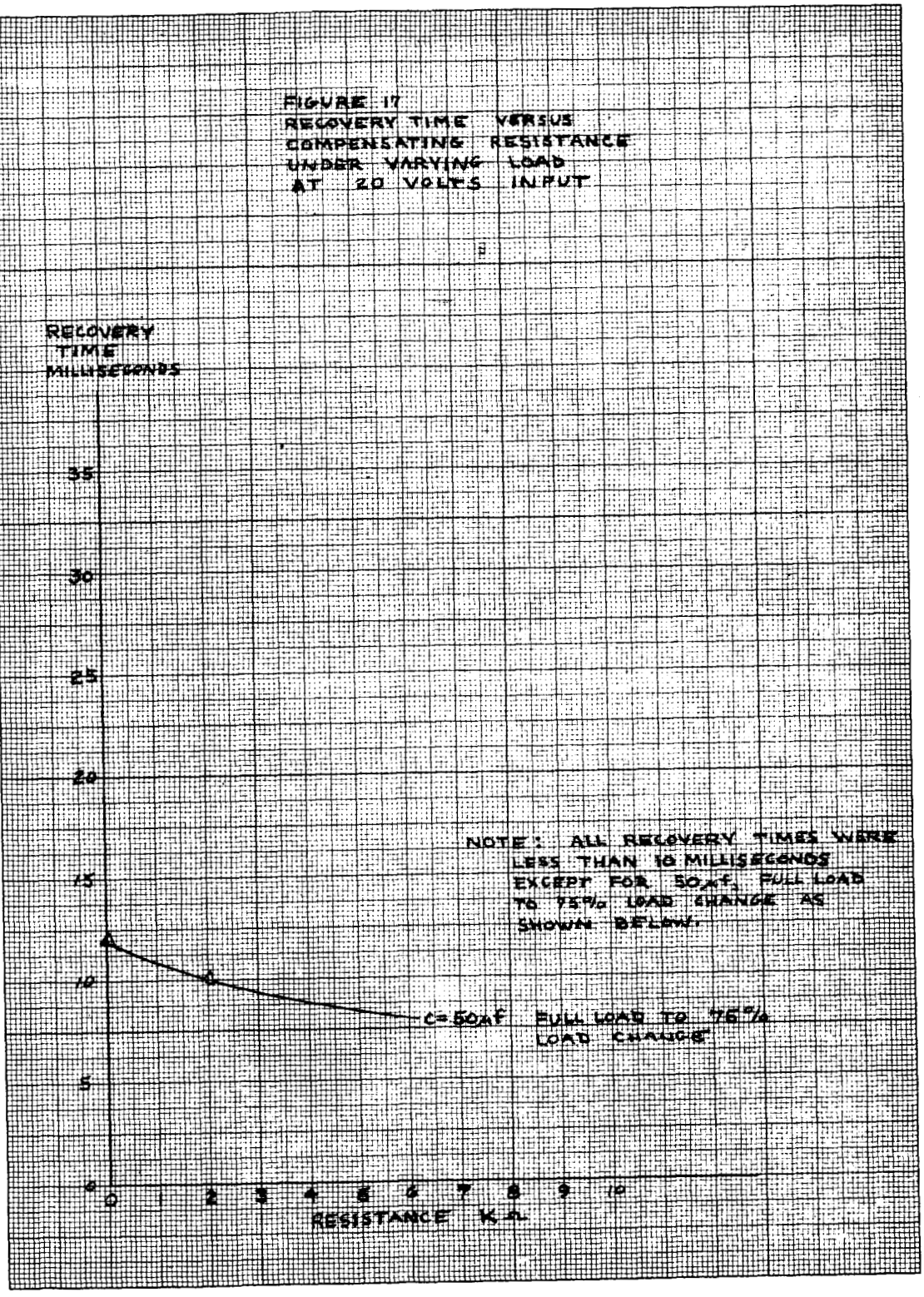


FIGURE 18
RECOVERY TIME VERSUS
COMPENSATING RESISTANCE
UNDER VARYING LOAD
AT 10 VOLTS INPUT